Claims:

1. A porous polishing pad useful for polishing semiconductor substrates, the porous polishing pad having a porous matrix formed from a coagulated polyurethane and a non-fibrous polishing layer, the non-fibrous polishing layer having a polishing surface with a pore count of at least 500 pores per mm^2, the pore count decreasing with removal of the polishing layer and the polishing surface having a surface roughness Ra between 0.01 and 3 μm.

2. The porous polishing pad of claim 1 wherein the pore count is 500 to 10,000 pores per mm^2.

3. The porous polishing pad of claim 2 wherein the surface roughness Ra is between 0.1 and 2 μm.

4. The porous polishing pad of claim 1 wherein the porous structure is a polyetherurethane polymer with polyvinyl chloride.

5. A method of preparing a porous polishing pad formed from a coagulated polyurethane, the porous polishing pad being useful for polishing semiconductor substrates, comprising:

supporting the porous polishing pad with a platen, the porous polishing pad having an upper surface and pore count per mm^2 that decreases below the upper surface;

applying a cutting tool to the upper surface of the top porous layer; and

removing the upper surface with the cutting tool to provide a polishing surface of a non-fibrous polishing layer, the polishing surface having a surface roughness Ra between 0.01 and 3 μm and having a pore count of at least 500 pores per mm^2 that decreases with removal of the polishing layer.

6. The method of claim 5, wherein the applying the cutting tool to the upper surface includes pressing a diamond conditioning head against the upper surface to provide the polishing layer with a surface roughness Ra between 0.1 and 2 μm.

7. The method of claim 5 wherein the removing the upper surface provides the polishing layer with the pore count of the polishing surface at 500 to 10,000 pores per mm^2.

8. A method of polishing a patterned semiconductor substrate including the step of polishing the semiconductor substrate with a porous polishing pad, the porous polishing pad having a porous matrix formed from a coagulated polyurethane and a non-fibrous polishing layer, the non-fibrous polishing layer having a polishing surface with a pore count of at least 500 pores per mm^2 and a surface roughness Ra between 0.01 and 3 μm.

9. The method of claim 8 wherein the porous polishing pad has a pore count per mm^2 that decreases below the polishing layer and including the additional step of maintaining the polishing surface with the pore count of at least 500 pores per mm^2 for at least 50 patterned wafers.

10. The method of claim 8 including the additional step of conditioning the porous polishing pad with a polymeric brush or polymeric pad.